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*Published in:*
2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)

*DOI (link to publication from Publisher):*
10.23919/EPE20ECCEEurope43536.2020.9215648

*Publication date:*
2020

*Document Version*
Accepted author manuscript, peer reviewed version

# Daisy Chain PN Cell for Multilevel Converter using GaN for High Power Density

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## Keywords

≪Multilevel converters≫, ≪Modulation strategy≫, ≪Gallium Nitride (GaN)≫, ≪High power density systems≫.

## Abstract

Power semiconductor devices are achieving high switching speed and high breakdown voltage. This improves inverter performance. But, as inverter improves, further challenge of $dv/dt$ noise is generated that needs to be tackled by filter stage. Multilevel inverters can solve this challenge. But there are implementation complexity associated with multilevel topologies like requirement of multiple isolated DC source, complicated charging algorithm, dedicated sensing hardware. This paper presents a switch capacitor type converter topology enabling a DC-AC three level output. Joining multiple iterations of topology in daisy-chained configuration, the converter can achieve voltage gain with multilevel waveform. Requirement of a single DC supply, with inherent charge balancing capability on capacitor, the topology is well suited for low voltage renewable sources like photovoltaic (PV) or fuel cell. The paper presents design of high frequency commutation loop. Utilizing finite element analysis (FEA) tool ANSYS Electronics Desktop (Q3D) to extract PCB parasitics helps in eliminating prototyping cost and time. Designed inverter is then subjected to continuous load test where it shows improving performance with increasing inductive load.

## Introduction

Wide bandgap (WBG) based semiconductor technology enables higher switch transition speed, leading to decreased losses in semiconductor devices. To take advantage of higher switching speed, the trend has been towards increasing switching frequency as it reduces output filter requirement. But a fast switching semiconductor device in itself is not going to be enough to achieve high density as it will be limited by passive components and cooling system [1]. In drives application high $dv/dt$ stress on output voltage can lead to motor bearing current and thus reduced lifespan of drive machines [2]. Also, increasing switching frequency will not continuously reduce output filter volume for grid connected inverters [3]. Focus needs to be directed towards different topological solutions as well. For example multilevel inverters can significantly reduce filter volume requirement without pushing $dv/dt$. In 80s fundamental works were published on multilevel converters [4]. Then in 90s and early 2000 saw the emergence of three most dominant multilevel topology, flying capacitor (FC), neutral point clamped (NPC), and modular multilevel converters ($M^2LC$) [5], [8]. Still, multilevel converter implementation is concentrated in high power, high voltage applications like high voltage DC (HVDC), medium voltage (MV) motor drives, and offshore wind turbine [6], [7]. To an extent this can be attributed to requirement of complex charge balancing algorithms alongwith additional voltage sensing and digital signal processor (DSP) per sub-module to maintain capacitor charge in multilevel topologies [9]. Furthermore, aforementioned multilevel topologies cannot be directly interfaced to renewable sources like photovoltaic (PV) panel, fuel

cell or battery storage applications. An intermediate boost converter is required to boost up low voltage supplied by renewable sources. New versions of multilevel topology are being introduced like modular multilevel series parallel converter (MMSPC) that can interface with low voltage supply but the charge balancing on each sub-module is similar to $M^2LC$ [10]. Work done in this paper is based on switched capacitor (SC) topology. For a long time switched capacitor topologies have been used for low power low voltage, regulated DC supply such as in CMOS integrated applications [13]-[14]. Due to high power density, SC have started gaining popularity in power electronics industry [15].

In this paper, a 5-level DC/AC multilevel inverter based on a topology called PN cell is presented. The topology, and its multiple variants is first introduced in [11]. In a recent publication [12], discussion is presented regarding working principle of PN cell. The publication then delves into converter dynamics by developing an averaged model of eight switch variant of the topology. The publication then proceeds with experimental demonstration of a two cell configuration.

The properties of a PN cell topology based multilevel inverter are,

1. Directly interfaces with low voltage DC supply like PV, fuel cell, battery storage systems.
2. Achieves high voltage gain without the use of magnetics.
3. Does not require additional charge balancing algorithm.
4. Produces multilevel waveform with $2n$+1 discrete levels, where $n$ is number of cells.

To illustrate the properties, focus of this paper will be on development of 5-level inverter. The inverter consists of two cell configuration with an input voltage of 40V. Discussion is presented on the importance of reducing resistance of capacitor charge path. In next section three variant of multilevel operation is shown as the topology is capable of producing different modulation schemes. To address the challenge of multiple power supplies for gate drivers and their dependence on cell capacitor, this paper contributes with a novel startup scheme. The startup scheme utilizes eHEMT's reverse conduction for charging the cell capacitor from OFF state. And finally, discussion on hardware development and experimental results are given.

## Three level topology - PN cell

In this paper a 6-switch variant of the PN cell topology is utilized. As explained in [12], a single PN cell produces 3-level waveform using operation states termed as P, N, and 0-state. Duty cycle for P-state is $d_\mathrm{P}$, and duty cycle for N-state is $d_\mathrm{N}$. During 0-state ($d_0$) cell capacitor is connected to the cell input terminal, charging back to input voltage level. The three duty cycles are related as $d_\mathrm{P} + d_\mathrm{N} + d_0 = 1$. Operation of a single PN cell in these states is shown in Fig. 1.

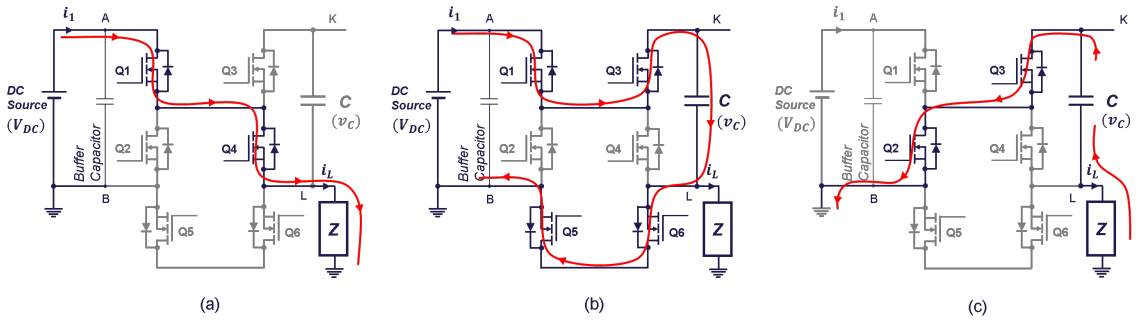


Fig. 1: Single PN cell operation in (a) P-state, (b) 0-state, and (c) N state

Because of inherent charge balancing capability of PN cell, the capacitor ($C$) maintains its voltage approximately equal to DC link voltage. Therefore output AC voltage across load is expressed by (1),

$$v_\mathrm{AC} = m \cdot V_\mathrm{DC} \cdot \sin(\omega t) \tag{1}$$

Where $m$ is modulation index and $V_{\mathrm{DC}}$ is cell input voltage. Utilizing the averaged model, [12] has explored the converter cell dynamics. It was shown that the 0-state resistance impacts converter performance. This behavior is apparent when looking at the input terminal current ($i_1$) in Fig. 1. Input terminal provides load current during P-state and charges capacitor ($C$) during 0-state. Input current ($i_1$), thus can be shown to consist of two parts (2).

$$i_1 = d_{\mathrm{P}} \cdot i_{\mathrm{L}} + \frac{(1 - d_{\mathrm{P}} - d_{\mathrm{N}})(V_{\mathrm{DC}} - v_{\mathrm{C}})}{4R_{\mathrm{DS(on)}} + R_{\mathrm{PCB}}} \tag{2}$$

where,

$$d_{\mathrm{P}} = \begin{cases} m \cdot \sin(\omega t) & \in \quad [0, \pi] \\ 0 & \in \quad (\pi, 2\pi] \end{cases} \qquad d_{\mathrm{N}} = \begin{cases} 0 & \in \quad [0, \pi] \\ m \cdot \sin(\omega t + \pi) & \in \quad (\pi, 2\pi] \end{cases} \tag{3}$$

$$i_{\mathrm{L}} = m \frac{V_{\mathrm{DC}}}{\sqrt{2}|Z|} \sin(\omega t) \in \quad [0, 2\pi] \quad \text{where,} \quad |Z| >> R_{\mathrm{DS(on)}} \tag{4}$$

Substituting (3) - (4) in (2) we obtain.

$$i_1 = \overbrace{m^2 \sin(\omega t) \cdot \frac{V_{\mathrm{DC}}}{\sqrt{2}|Z|} \sin(\omega t)}^{\textit{load dependent}} + \overbrace{\Big(1 - m|\sin(\omega t)|\Big) \frac{V_{\mathrm{DC}} - v_{\mathrm{C}}}{4R_{\mathrm{DS(on)}} + R_{\mathrm{PCB}}}}^{\textit{capacitor charge}} \tag{5}$$

$R_{\mathrm{PCB}}$ is PCB trace parasitic resistance during 0-state. (5) indicates that DC input current to the inverter has two components, one is dependent directly on the load and second component is dependent on capacitor voltage difference from the input voltage. This second component is an additional load to the cells that generate loss. In order to achieve good performance, capacitor charge component needs to be minimized. As can be seen from (5), if the capacitor voltage ($v_{\mathrm{C}}$) drops much lower than input DC link voltage, ($V_{\mathrm{DC}} - v_{\mathrm{C}}$) becomes large invoking higher input current. One key factor in maintaining capacitor voltage close to DC link voltage is RC time constant ($\tau$), formed by $R_{\mathrm{DS(on)}} + R_{\mathrm{PCB}}$, and $C$. As the capacitor gets charged during 0-state of switching period. It is important to make sure that even at max. modulation index ($m_{\max}$), RC time constant ($\tau$) is smaller than 0-state time (6).

$$R_{\mathrm{DS(on)}} + R_{\mathrm{PCB}} < \frac{1 - m_{\max}}{k \cdot f_{\mathrm{sw}} \cdot C} \quad \text{where,} \quad k \in [3, 5] \tag{6}$$

$R_{\mathrm{PCB}}$ is dependent on size of PCB, which is determined by the device footprint and gate driver circuit. Gallium nitride (GaN) based devices exhibit improved performance over silicon counterparts in a smaller package. Lateral GaN eHEMT device (GS61008P) used in this paper is a 100V-90A device and has an on-state resistance of 7m$\Omega$ [16].

## Modulation strategy in multicell inverter

When more than one cell is daisy chained it creates possibility to obtain multilevel waveform of $2n+1$ levels where $n$ is number of cells. The topology also has potential to produce standard 3-level waveform. In Fig. 2, two cell configuration in daisy chain is shown to operate in three different states marked as (I), (II), (III). These three operation states are marked accordingly on the different modulation schemes presented in Fig. 2. The flexibility to operate each cells independently gives this topology the potential to produce various modulation schemes. DC link voltage for the simulation shown is 50V.

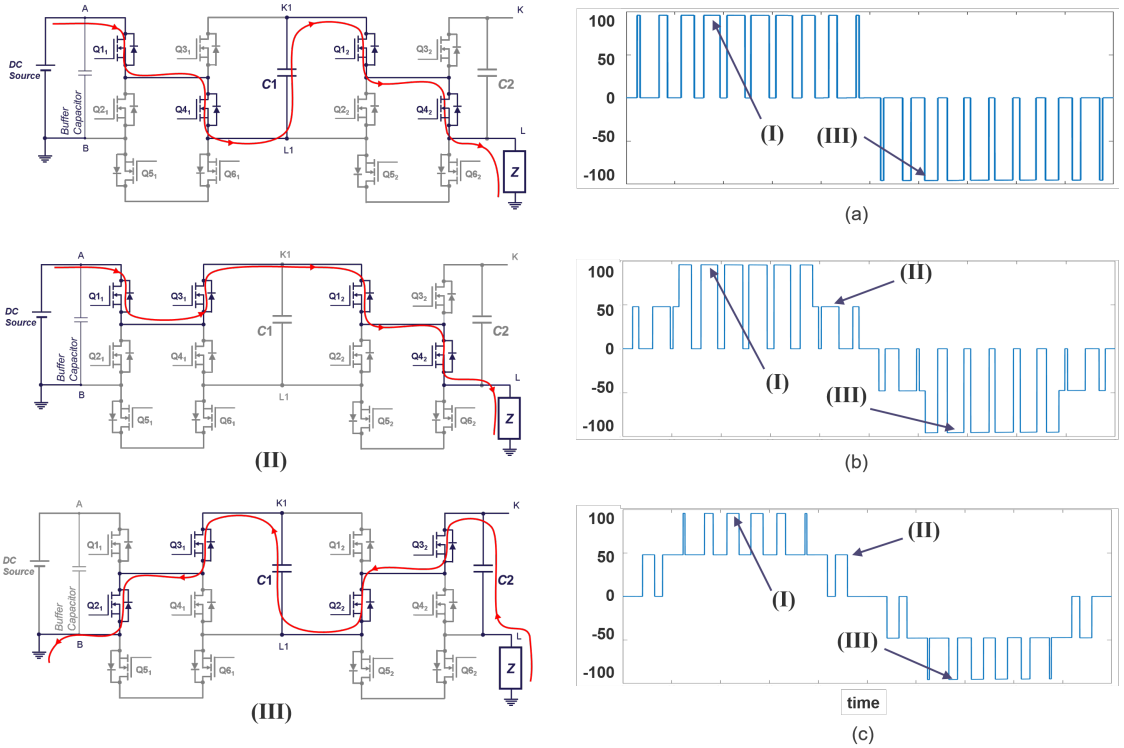


Fig. 2: Output voltage at different modulation strategy (a) 3-level waveform, (b) modified 5-level, and (c) standard 5-level output waveform

Modulation strategy 1 is achieved when all the cells are synchronized in their operation states. Therefore, the capacitors to each cell get charged and discharged together. This modulation is simpler to implement as each cell gets same signal from the controller. Also the modulation is achieved by using a single carrier (triangular) signal compared to a modulating (sinusoidal) signal. With strategy (a) the converter does not provide the advantages of multilevel waveform. Modulation strategy shown in (b), is a modification of strategy (a) where capacitor of each cell are still charged in sync, thus maintaining low ripple current on the capacitors. Finally modulation strategy (c) provides multilevel operation where the variation of voltage at each switching instant is equal to input DC link voltage. Modulation strategy in (c) is achieved using phase disposition of multiple carrier [17]. In the current two cell configuration, two carriers are used which are phase shifted by $\phi = T_{SW}/2$, where $T_{SW}$ is switching period. Because of phase shift in operation states of the two cells, capacitor charging of the cells are not synchronized unlike the previous two schemes. This leads to higher capacitor ripple current compared to strategy (a) and (b).

## Design and Optimization of Power Loop

Power PCB in this paper is designed in conjunction to SPICE simulation platform. SPICE simulation model is used as a digital twin of the actual PCB. For this purpose finite element analysis (FEA) method is employed on each iteration of PCB designed. ANSYS Electronics Desktop (Q3D) is used to extract the parasitic of copper layers which is then fed back into SPICE model to analyze design performance. Necessary changes are made depending on these simulation results [18]. Digital twin methodology accelerates hardware development process by eliminating prototyping cost and time which is a major push by industry. While using this methodology it is important to first identify high frequency commutation loops. Referring to operation states of PN cell. During positive half-cycle of fundamental frequency when inverter is modulating between P-state and 0-state, a high frequency commutation loop is observed on the output side of inverter shown in Fig. 3(a).

During negative half-cycle of fundamental frequency a similar high frequency commutation loop will emerge on the input side of PN cell. Both these loops are identical to power loop present in voltage

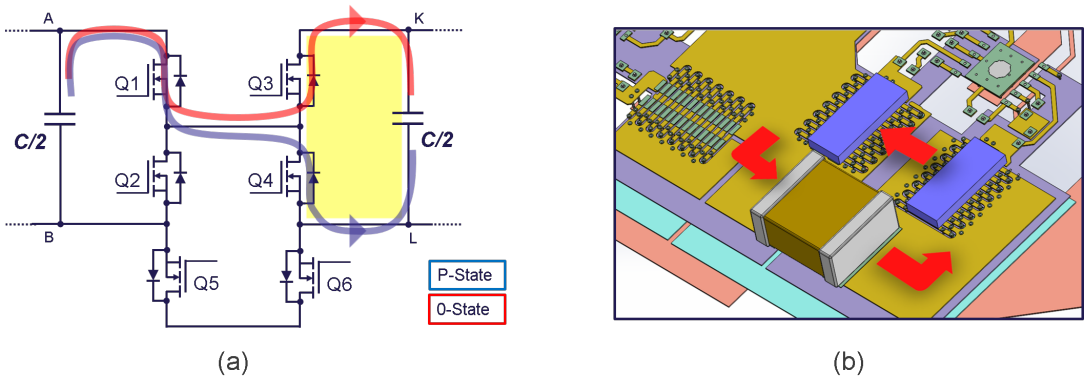


Fig. 3: (a) High frequency commutation loop on the output side of PN cell during positive half-cycle of fundamental frequency, and (b) lateral layout design for the commutation loops

source converters (VSCs) between DC-link capacitor and half-bridge. Two most conventional layout for commutation loop are considered - vertical and lateral layout [19]. For vertical layout most optimum performance is achieved when close PCB layers are utilized for return path of loop. Lateral layout is usually contained within either top or bottom PCB layer. In this paper, it was observed that employing multiple internal layers for switch node and paralleled vias results in lateral layout performing better than vertical layout design. A 3-dimensional render of lateral layout is presented in Fig. 3(b).

Using the FEA method, loop inductance for lateral layout is calculated to be 0.42nH. This value consists of the partial self-inductance of individual trace as well as their mutual inductance based on spatial arrangement. Loop inductance value calculated using FEA is then exported as matrix into SPICE simulation. For the GaN eHEMT devices SPICE model is utilized from manufacturer that includes package inductance. The device is kept at 25°C. Gate resistance of 6Ω is used for both high side and low side devices. Using a double pulse test, comparison between simulation (utilizing FEA extracted values) and experimental waveform is provided. Turn ON and turn OFF transients are shown in Fig. 4. Switching transient speed as well as voltage overshoot during turn-off instant for low side HEMT ($Q2$) matches closely between simulation and experimental observation. Although, simulation results oscillations sustain for longer compared to experimental results but results have been successful in validation design methodology utilizing digital twin. Calculating the switch transient speed and voltage overshoot, device is switched at 21A drain current. Turn-off speed of 6ns is measured with $dv/dt$ of 6V/ns. Peak measured voltage of 53V gives an overshoot ($\Delta$V) of 13V which is a 33% overshoot. For turn-on, a speed of 7.5ns is observed which gives a dv/dt of 4.8V/ns.

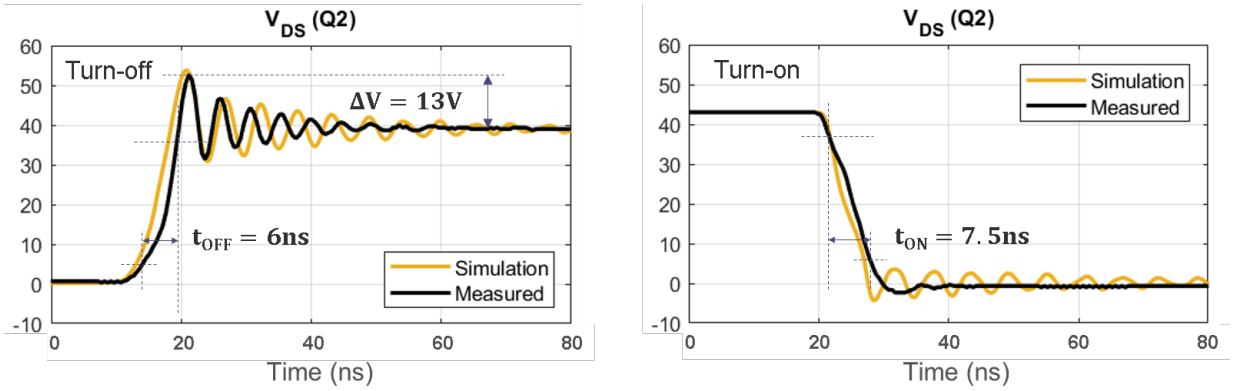


Fig. 4: Voltage surge measurement during double pulse test on low side HEMT in simulation and experimentation

## Result

Designed inverter that contains two cells is shown in Fig. 5. Power board contains six switches of each cell, their drivers and output capacitor. Cell 1 has been marked in the figure. A separate PCB is attached to power board, which feeds signal to gate drivers. This second PCB is termed as Controller board. Controller board houses signal isolation circuit as well as a DC-DC circuit to power gate drivers. Although in the current iteration of hardware the controller board is designed to be in perpendicular to the power board for ease of access during debugging. The controller board can be designed to float in parallel to power board, reducing volumetric dimension of the hardware. Fig. 5 shows additional electrolytic capacitors that are added because the multilayer ceramic capacitors (MLCC) were not enough to sustain the capacitor voltage at high load.

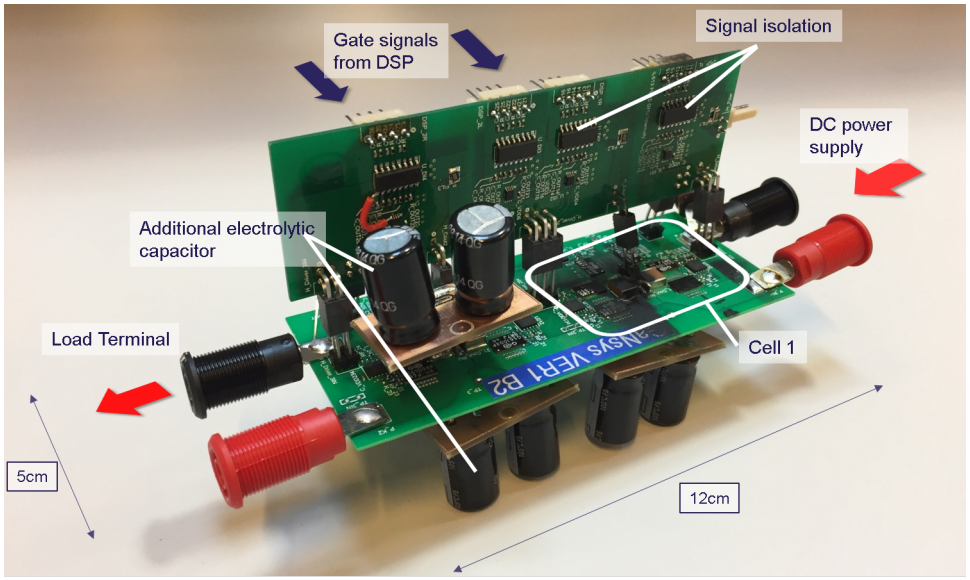


Fig. 5: Power Board and Controller Board fabricated and assembled

### Startup sequence

In order to eliminate the requirement of high number of isolated DC-DC regulators or flyback transformer based design to power up gate drivers. An approach is taken where capacitors ($C$) is used as power source for a non-isolated DC-DC circuit that can convert 40V to regulated 5V supply to be used by gate drivers. But with this interdependent design, challenge arises to charge the capacitors ($C$) when starting from OFF state. In order to solve this issue, eHEMT's reverse conduction is used. In Fig. 6 a two step process is shown to charge capacitor of cell 1 and cell 2 in a sequential process. At first, when only DC link voltage is available switch $Q1_1$ and $Q5_1$ is supplied with a constant 20% duty cycle to charge up capacitor $C1$ using reverse conduction of $Q3_1$ and $Q6_1$. At this stage, capacitor $C1$ provides power to gate drivers of switch $Q1_2$ and $Q5_2$ of cell 2. And in a similar manner capacitor $C2$ is charged. This two stage concept for the two cell configuration is shown in Fig. 6.

Likewise, if there are more cells, same methodology is capable of charging up capacitors for each cell in a subsequent manner.

### Inverter operation under load

At an input DC source voltage of 40V, inverter is tested under load with various power factor. With increasing inductance, power angle is raised from $7^\circ \rightarrow 20^\circ \rightarrow 29^\circ$ at $\approx 20\Omega$ load impedance. DC link voltage is kept at 40V with a modulation index of 0.65 at 15kHz switching frequency. Cell capacitance $C1 = 700\mu$F and $C2 = 350\mu$F. Input and output waveforms are shown in Fig. 7. RMS value of inverter input current, output voltage and output current for the three cases shown in Fig. 7 is given in Table I. The RMS value is calculated using RMS function in MATLAB on the acquired waveform. There is

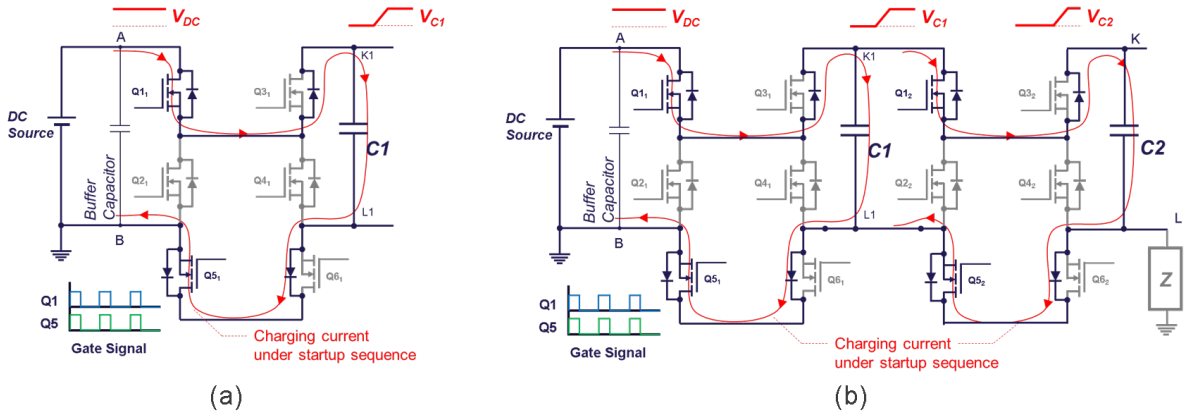


Fig. 6: Startup sequence with (a) capacitor $C1$ of cell 1 getting charged to DC link voltage, (b) capacitor $C2$ getting charged

approximately 2W of losses by the gate driver, its power supply, and signal isolation circuit at 15kHz switching frequency. Efficiency given in Table I has been adjusted for this additional loss and thus represents purely the DC to AC power conversion efficiency. The current hardware's power handling is limited by its heat dissipation capability and therefore with proper thermal design power rating can be increased.

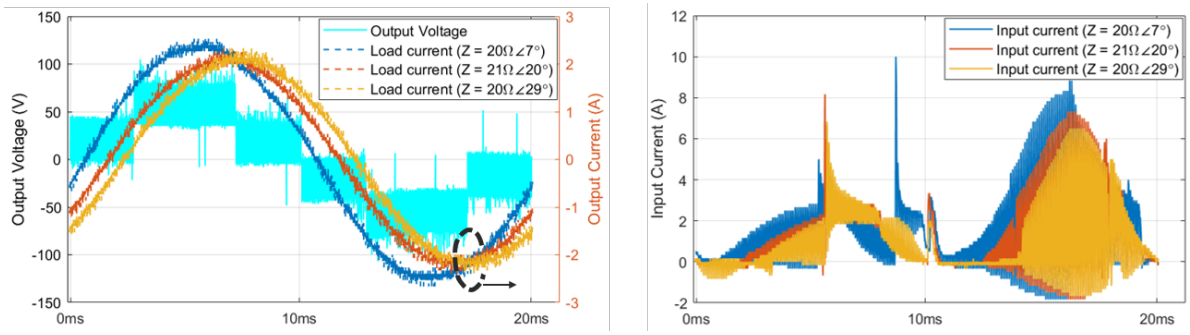


Fig. 7: (a) Inverter output voltage and load current, (b) Input current

Decreasing input current with increasing inductive load shown in Fig. 7(b), can be explained using (5). In [12], experimental demonstration with increased inductive load shows smaller capacitor voltage variation. According to (5), if capacitor voltage variation is decreased, inverter input current decreases and therefore delivers better performance.

Table I: Two cell configuration performance under increasing inductive load

| Load Impedance | Input current | Output Voltage | Output Current | Efficiency |
|---|---|---|---|---|
| 20Ω ∠7° | 2.3 A | 38 V | 1.7 A | 71.7 % |
| 21Ω ∠20° | 1.9 A | 39 V | 1.5 A | 79.1 % |
| 20Ω ∠29° | 1.7 A | 39 V | 1.5 A | 88.6 % |

The developed hardware is also subjected to purely inductive load. In previous test results, input current during the negative half-cycle of fundamental frequency was highest. In the purely inductive load case however, input current during negative cycle of line frequency is negligible. Output waveform and input current for the purely inductive load is shown in Fig. 8.

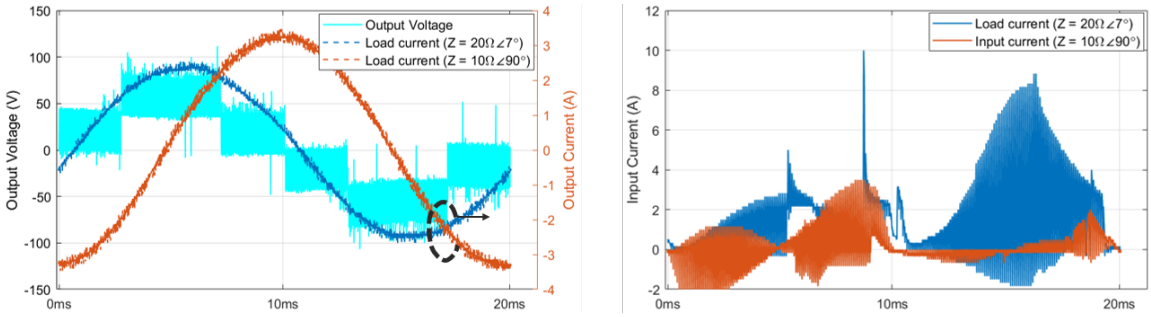


Fig. 8: (a) Inverter output voltage and load current, (b) Input current

## Conclusion

This paper has presented PN cell topology based 5-level inverter. This work aimed towards interfacing directly to a low voltage supply, therefore the designed inverter is based on two cell configuration with a 40V DC input voltage. The inverter can be extended to higher number of levels by adding more cells and thus producing higher output voltage that can be interfaced with grid or drive applications. A startup scheme is proposed that utilizes reverse conduction of eHEMT device to charge cell capacitor from complete OFF state. The converter is then subjected to double pulse test. Turn-off time is measured to be 6ns with dv/dt of 6V/ns at 21A drain current. Conformation between simulation and experiment results during voltage transients helps in reducing prototyping cost and time. This digital twin methodology can be used for novel topology or module design where significant amount of literature is not available. Finally, the two cell inverter is operated under varying load conditions.

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